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09/510,300	02/22/2000	Sung-Il Park	8733.20044	2217

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EXAMINER	
DUONG, THOI V	

ART UNIT	PAPER NUMBER
2871	

DATE MAILED: 04/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/510,300	PARK ET AL.	
	Examiner	Art Unit	
	Thoi V. Duong	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 January 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* ~~is~~/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* ~~is~~/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1104*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on January 27, 2005 has been entered.

Accordingly, claims 1, 6, 10, 15 and 20 were amended, and new claim 21 was added. Currently, claims 1-21 are pending in this application.

Response to Arguments

2. Applicant's arguments with respect to claims 1, 6, 10, 15 and 20 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting

directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

4. Claims 1, 3, 4 and 21 are rejected under 35 U.S.C. 102(e) as being anticipated by Shimada et al. (Shimada, USPN 5,877,830).

Re claim 1, as shown in Figs. 1-3, Shimada discloses a liquid crystal display (LCD) comprising:

a gate line 2 on a first transparent substrate 1a,

a data line 8 arranged to cross the gate line wherein the gate line is insulated from the data line,

a gate electrode 2a protruding from said gate line 2 in an area where said data line crosses said gate line,

a thin film transistor having a source electrode 7a connected to the data line 8 and a drain electrode 7b separated from the source electrode,

a passivation layer 9 covering the thin film transistor wherein a contact hole 10 exposing a portion 7c of the drain electrode is formed in the passivation layer 9, and

a pixel electrode 11 formed on the passivation layer 9, the pixel electrode 11 being connected to the drain electrode through the contact hole 10 and partially overlapping the data line 8;

a black matrix 13, a color filter 14 and a common electrode 15 on a second transparent substrate 12a, the black matrix 13 partially overlapping the data line 8 (Fig. 1); and

liquid crystals 17 provided and sealed between the first and second transparent substrates (col. 8, lines 16-19),

wherein, re claims 3 and 4, the passivation layer is an organic passivation layer made of acryl (col. 7, lines 1-5); and

wherein, re claim 21, as shown in Fig. 1, a portion of the black matrix 13 that partially overlaps the data line 8 has a width of about 1 micrometer or more, which is equal to the overlap width of the pixel electrode 11 and the data line 8 (col. 9, lines 65-67).

5. Claims 15-17 are rejected under 35 U.S.C. 102(a) as being anticipated by Hanazawa et al. (Hanazawa, USPN 5,953,088).

Re claim 15, as shown in Figs. 12 and 15, Hanazawa discloses a method of fabricating a liquid crystal display having a transparent substrate 60 on which a gate line region and a data line region are defined, comprising:

simultaneously forming a gate line 62 in the gate region wherein a gate electrode 63 protrudes from the gate line, and a cut-off film 53a(SH);

forming a data line 50a(X) in the data line region on the transparent substrate, wherein the data line crosses and is insulated from the gate line, and wherein a source electrode 50a(X) is formed at one side of the data line, and wherein a drain electrode 78 is formed which confronts and is isolated from the source electrode;

forming a passivation layer 81 covering the gate fine region, the data line region and the cut-off film, wherein a contact hole 80 exposing a portion of the drain electrode is formed in the passivation layer (Fig. 12); and

forming a pixel electrode 51(PE) connected to the drain electrode through the contact hole on the passivation layer (Fig. 12), the pixel electrode partially overlapping the data line 50a(X),

wherein an edge portion of the cutoff film 53a(SH) is overlapped by an edge portion of the data line 50a(X), and the edge portion of the cutoff film 53a(SH) and the edge portion of the data line 50a(X) are substantially coextensive with the pixel electrode 51(PE) (see Fig. 15 below);

wherein, re claim 16, the passivation layer is an organic passivation layer (col. 5, lines 63-67); and

wherein, re claim 17, the cut-off film 53a(SH) and the gate line 62 are formed on a same level (Figs. 11 and 12).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shimada et al. (Shimada, USPN 5,877,830) in view of Kobayashi et al. (Kobayashi, USPN 5,847,792).

Shimada discloses a liquid crystal display includes all that is recited in claim 2 except for a location of the black matrix which is selected according to a direction of rubbing an alignment film.

As shown in Figs. 19A and 19B, Kobayashi discloses a LCD comprising a black matrix 35, a common electrode 12 and an alignment film on a counter substrate 2, wherein the black matrix is formed in regions on the counter substrate opposed to the regions in which inversely tilted domains are apt to be caused to prevent light leakage (col. 12, lines 50-53 and col. 13, lines 50-59).

Thus, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the LCD of Shimada with the teaching of Kobayashi by selecting a location where the black matrix overlaps the data line according to a direction of rubbing an alignment film to prevent leakage current due to photoelectromotive force (col. 13, lines 57-59).

8. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shimada et al. (Shimada, USPN 5,877,830) in view of den Boer et al. (den Boer, USPN 5,641,974).

Shimada discloses a liquid crystal display that is basically the same as that recited in claim 5 except for an organic passivation layer made of BCB. As shown in Figs. 1 and 7, den Boer discloses that a photo-imageable material such as BCB is to be used to form the insulating layer 33 for the purpose of reducing capacitive cross-talk between the pixel electrode 3 and the data line 5 in overlap area 18 (col. 6, lines 1-9).

Thus, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the LCD of Shimada with the teaching of den Boer by forming the organic passivation layer of BCB to reduce capacitive cross-talk in the overlap area of the pixel electrode and the data line (col. 6, lines 1-9).

9. Claims 6, 8, 9 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jung (USPN 6,300,987 B1) in view of Yoshino (USPN 5,358,810).

Re claim 6, as shown in Figs. 6 and 7, Jung discloses a liquid crystal display (LCD) comprising:

a thin film transistor plate further comprising:

a gate line 210 on a first transparent substrate 100;

a first data line 310 (on left of Fig. 7) arranged to cross the gate line 210 wherein the gate line is insulated from the data line;

a gate electrode 110 protruding from said gate line in an area where said data line crosses said gate line;

a thin film transistor 410 having a source electrode 313 connected to the first data line and a drain electrode 312 separated from the source electrode;

a passivation layer 350 covering the thin film transistor wherein a contact hole exposing a portion of the drain electrode 312 is formed in the passivation layer 350; and

a pixel electrode 510 on the passivation layer and being connected to the drain electrode 312 through the contact hole, wherein the pixel electrode 510 partially overlaps the first data line 310 at a first end of the pixel electrode 510 by a width of W1 (Applicant's a width of "b"),

wherein the pixel electrode 510 partially overlaps a second data line 310 at a second end of the pixel electrode (on right of Fig. 7) opposite to the first end by a width

of W3 (Applicant's a width of "a"), and wherein "a" and "b" are not equal (col. 5, lines 31-50).

Re claim 8, Jung discloses that an overlap width between the pixel electrode 510 and the first data line 310 is selected according to a direction R of rubbing an alignment film as shown in Fig. 7 (col. 3, lines 31-50).

Re claim 9, the passivation layer 350 is an organic passivation layer)col. 4, lines 64-67).

Re claim 19, Jung discloses that a first overlap width W1 between the first data line and the pixel electrode is larger than a second overlap width W3 between the pixel electrode and the second data line (col. 5, lines 31-40).

Jung discloses a LCD that is basically the same as that recited in claim 6 except for a second transparent substrate comprising a color filter plate including a black matrix, a color filter and a common electrode.

As shown in Figs. 2 and 3E, Yoshino discloses a liquid crystal display comprising a thin film transistor substrate 4 and a color filter plate 2 comprising a color filter 36, a black matrix 24 and a common electrode 12 (col. 3, lines 33-42 and col. 4, lines 22-24), wherein liquid crystals is provided and sealed between betweenthe thin film transistor substrate 4 and the color filter plate 2 (col. 5, line 66 through col. 6, line 4).

Thus, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the LCD of den Boer with the teachings of Yoshino by forming a second transparent substrate comprising a color filter plate

including a black matrix, a color filter and a common electrode so as to realize a color display having a sufficient light-shielding effect (col. 2, lines 25-29 and 43-46).

10. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Jung (USPN 6,300,987 B1) in view of Yoshino (USPN 5,358,810) as applied to claims 6, 8, 9 and 19 above, and further in view of Shimada et al. (Shimada, USPN 5,877,830).

The LCD of Jung as modified in view of Yoshino above includes all that is recited in claim 7 except for an overlap width between the pixel electrode and the first data line being between 2 micrometer and 4 micrometer, and an overlap width between the pixel electrode and the second data line is less than 2 micrometer.

As shown in Fig. 4, Shimada discloses that the overlap width of the pixel electrode 11 and the data line 8 is about 1 micrometer or more to perform a display without crosstalk (col. 9, lines 58-67). Accordingly, it is obvious that with the teaching of Shimada, an overlap width W1 between the pixel electrode and the second data line of Jung can be formed about 1 micrometer and an overlap width W3 between the pixel electrode and the first data line of Jung can be 2 micrometer or more since W1 is wider than W3.

Thus, it would have been obvious to one having ordinary skill in the art at the time the invention was made to further modify the LCD of Jung with the teaching of Shimada by forming an overlap width between the pixel electrode and the first data line being between 2 micrometer and 4 micrometer, and an overlap width between the pixel electrode and the second data line is less than 2 micrometer so as to perform a display without crosstalk (col. 9, lines 58-64).

11. Claims 10-12, 14 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hanazawa et al. (Hanazawa, USPN 5,953,088) in view of Murade (USPN 6,388,721 B1).

Re claims 10 and 20, as shown in Figs. 5, 12 and 15, Hanagawa discloses a LCD comprising:

a thin film transistor plate 83 further comprising:

a gate line 62 on a first transparent substrate 60 (col. 3, lines 45-48),

a data line 50a(X) arranged to cross the gate line wherein the gate line is insulated from the data line,

a gate electrode 63 protruding from said gate line in an area where said data line crosses said gate line,

a thin film transistor TR having a source electrode 50a(X) connected to the data line and a drain 78 separated from the source electrode wherein the source and drain electrodes confront each other,

a passivation layer 81 covering the thin film transistor wherein a contact hole 82 exposing a portion of the drain electrode is formed in the passivation layer, and

a pixel electrode 51 (PE) formed on the passivation layer and being connected to the drain electrode through the contact hole (Fig. 12), wherein the pixel electrode partially overlaps the data line;

a color filter plate 87 including a color filter 85 and a common electrode 86 on a second transparent substrate 84 (col. 3, lines 59-63); and

liquid crystals 90 injected and sealed between the thin film transistor plate and the color filter plate,

wherein a cut-off film 53a(SH) is formed under the data line 50a(X), an edge portion of the cutoff film 53a(SH) is overlapped by an edge portion of the data line 50a(X), and the edge portion of the cutoff film 53a(SH) and the edge portion of the data line 50a(X) are substantially coextensive with the pixel electrode 51(PE) (see Fig. 15 below).

wherein, re claim 11, the passivation layer is an organic passivation layer (col. 5, lines 63-67);

wherein, re claim 12, the cut-off film 53a(SH) and the gate line 62 are formed on a same level (Figs. 11 and 12); and

wherein, re claim 14, the cut-off film 53a(SH) is formed at one side of the data line, said side selected according to a direction of rubbing an alignment film (Fig. 10 and col. 7, lines 40-61).

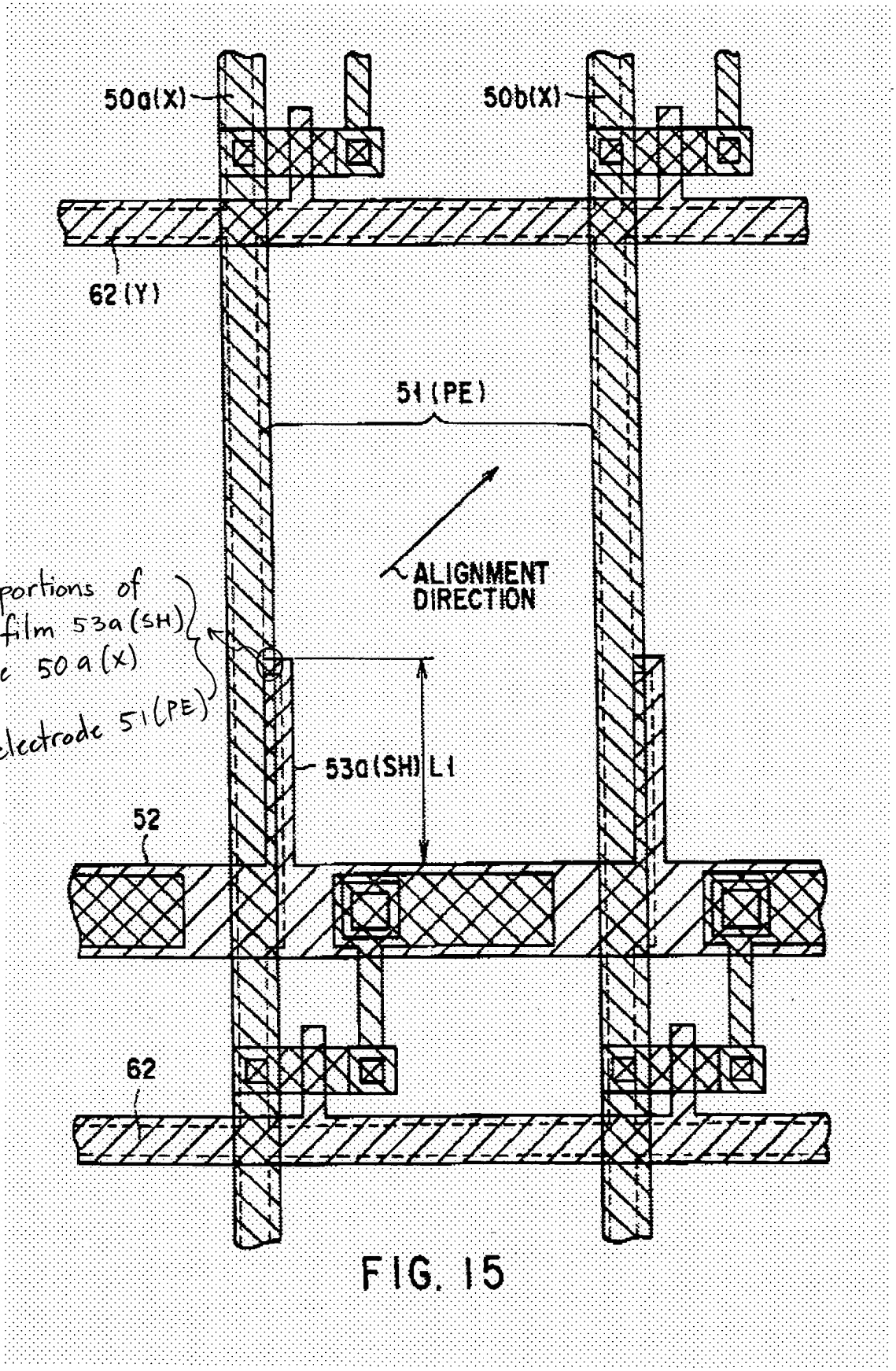
50a(X)
50b(X)
62(Y)
51(PE)
ALIGNMENT DIRECTION
Edge portions of cut-off film 53a(SH) data line 50a(X) and pixel electrode 51(PE)
53a(SH)
L1
52
62

FIG. 15

Hanazawa discloses a LCD that is basically the same as that recited in claims 10 and 20 except for a black matrix formed on the color plate.

As shown in Fig. 20, Murade discloses a LCD comprising a black matrix 6 formed on a second substrate 31, a pixel electrode 14, a data line 2, and a cut-off film 7 formed under the data line and overlapped by the data line and the pixel electrode.

Thus, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the LCD of Hanazawa with the teaching of Murade by forming a black matrix on the second substrate so as to prevent the display from being directly exposed to light and hence to obtain high quality images (col. 6, lines 16-27).

12. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hanazawa et al. (Hanazawa,USPN 5,953,088) in view of Murade (USPN 6,388,721 B1) as applied to 10-12, 14 and 20 above and further in view of Shimada et al. (Shimada, USPN 5,877,830).

As shown in Fig. 15 of Hanazawa, an overlap region between the pixel electrode 51(PE), the cut-off layer 53a(SH) and the data line 50a(X) has a same width. However, Hanazawa does not disclose the overlap region between the pixel electrode, the cut-off layer and the data line having a width of between 2 micrometer and 4 micrometer as recited in claim 13.

As shown in Fig. 4, Shimada discloses that the overlap width of the pixel electrode 11 and the data line 8 is about 1 micrometer or more for performing a display without crosstalk (col. 9, lines 58-67).

Thus, it would have been obvious to one having ordinary skill in the art at the time the invention was made to further modify the LCD of Hanazawa with the teaching of Shimada by forming an overlap region between the pixel electrode, the cut-off layer and the data line range having a width of between 2 micrometer and 4 micrometer so as to perform a display without crosstalk (col. 9, lines 58-67).

13. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hanagawa et al. (Hanazawa, USPN 5,953,088) in view of Shimada et al. (Shimada, USPN 5,877,830).

As shown in Fig. 15 of Hanazawa, an overlap region between the pixel electrode 51(PE), the cut-off layer 53a(SH) and the data line 50a(X) has a same width. However, Hanazawa does not disclose the overlap region between the pixel electrode, the cut-off layer and the data line having a width of between 2 micrometer and 4 micrometer as recited in claim 13.

As shown in Fig. 4, Shimada discloses that the overlap width of the pixel electrode 11 and the data line 8 is about 1 micrometer or more for performing a display without crosstalk (col. 9, lines 58-67).

Thus, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the LCD of Hanazawa with the teaching of Shimada by forming an overlap region between the pixel electrode, the cut-off layer and the data line range having a width of between 2 micrometer and 4 micrometer so as to perform a display without crosstalk (col. 9, lines 58-67).

Conclusion

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thoi V. Duong whose telephone number is (571) 272-2292. The examiner can normally be reached on Monday-Friday from 8:30 am to 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Kim, can be reached at (571) 272-2293.

Thoi Duong

04/08/2005

TARIFUR R. CHOWDHURY
PRIMARY EXAMINER